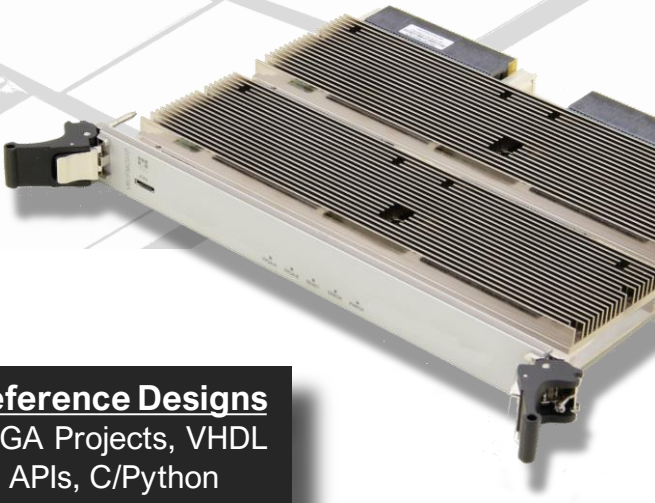
Hybrid DSP – Embedded Sensor Processing

Specialists in embedded processing boards and IP aligned with the SOSA Technical Standard for demanding defence, aerospace and industrial programs

Hardware Products
- *COTS 3U/6U VPX FPGA processing boards*
- *Modified-COTS and custom boards*
- *Integrated (3rd party) FMC solutions*
- *Designed and manufactured by Hybrid DSP in the Netherlands*
- *Reference designs included*

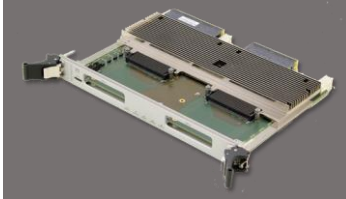
IP for 3rd party Board Designs
- *VITA46.11 IPMC and board management*
- *Firmware and software libraries*
- *Board reference designs (schematics / layouts)*

Services for OEM and System Integrators
- *System integration support*
- *Automated test equipment (ATE)*
- *Compliance and compatibility consultancy*
- *Product and lifecycle management*



OVERVIEW

Products
COTS

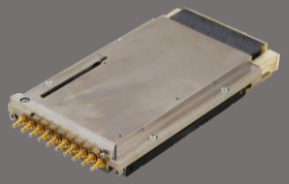


ATE
Hardware + Software

Reference Designs
FPGA Projects, VHDL
APIs, C/Python

C
PYTHON

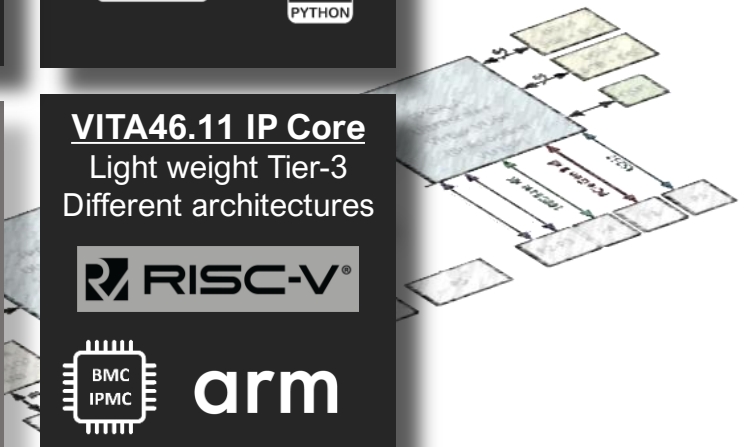
Products
Modified-COTS



Modular VPX / SOSA™ Aligned Solutions*

VITA46.11 IP Core
Light weight Tier-3
Different architectures

RISC-V
BMC IPMC
arm



Products
Integrated FMC Solutions

Services
Sales cycle support
Technical Consultancy

Services
Production Transfer
Product Management

AMD Adaptive Computing Partner SELECT

DESIGNED AND MANUFACTURED IN EUROPE

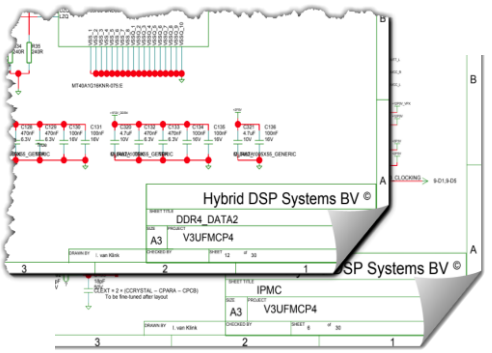
url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

VPX™ SOSA Sensor Open Systems Architecture

Kanaalpark 157
2321JW Leiden
The Netherlands

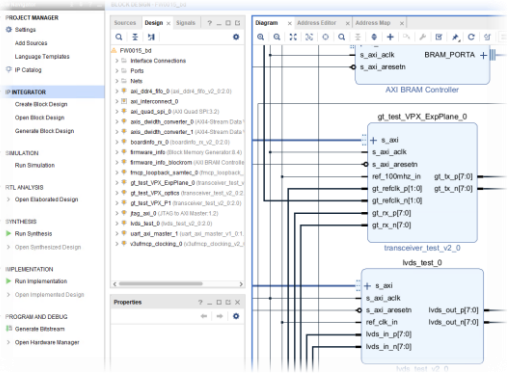
DESCRIPTION

COMPANY



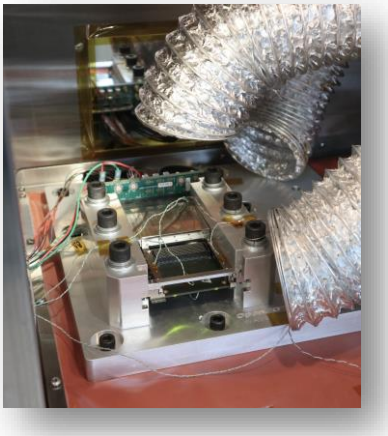
Hybrid DSP Systems was founded in the Netherlands in 2018. With more than 15 years experience, the team set out to provide system integrators with an efficient, secure and scalable service for the board level products that - for logistical or technical reasons - cannot be provided as Commercial Off The Shelf (COTS). In VPX systems this typically involves (RF) I/O and FPGA boards. Customers wish to reduce the overhead required for ensuring compliance and compatibility with the various standards and the rest of the system; as well as development, production and product management of these application specific boards.

Modified-COTS REALITY CHECK



Modified-COTS (M-COTS) seeks to strike a balance between COTS and the fully custom engineering services route. A COTS supplier can base a solution on a proven core design with a roadmap that is common to multiple derivative M-COTS boards. The customer specific requirements are then implemented, for instance: clocks, digitizers, waveform generators, optical transceivers, cooling solution, or production cost savings.

Unfortunately, the M-COTS development aspect frequently ends up in a no-man's land lost between the COTS product sales teams, the system integration sales team and the customer's technical groups.



The more critical and specific the M-COTS boards are to the overall success of the program, the more important it is to have the actual M-COTS development engineers involved in every step of the sales process. Ultimately, we end up missing the close detail driven collaboration between an engineering services company and the customer that outsources the custom board development. The apparent cost-savings can come at a price.

Hybrid DSP's scalable M-COTS service ensures your sales and technical teams always have access to the most up-to-date IP, documentation, change logs, project status and dynamic risk/cost analyses. We do all of this via secure private git repositories – and yes you can submit pull-requests, too. This reduces your and our overhead, lowers risk and maximizes the efficiency of in-person or video meetings.

CONTACT

Contact Hybrid DSP to discuss how we can accelerate your next development.

** Products and solutions were developed in alignment with the SOSA™ Technical Standard*

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2. The VPX logo and related marks are trademarks of VITA

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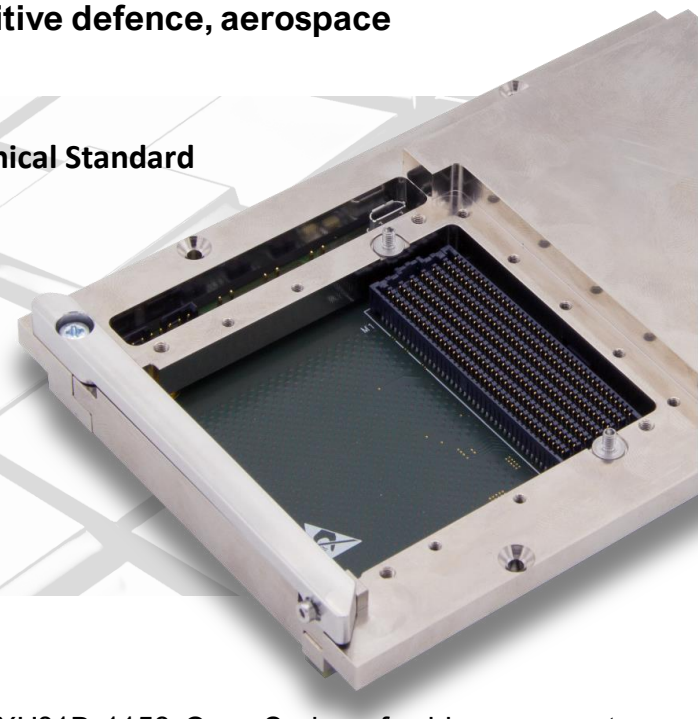
url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

V3UFMC01P AMD UltraScale FMC+ Carrier

Rugged mid-range FPGA processing for cost sensitive defence, aerospace and industrial programs



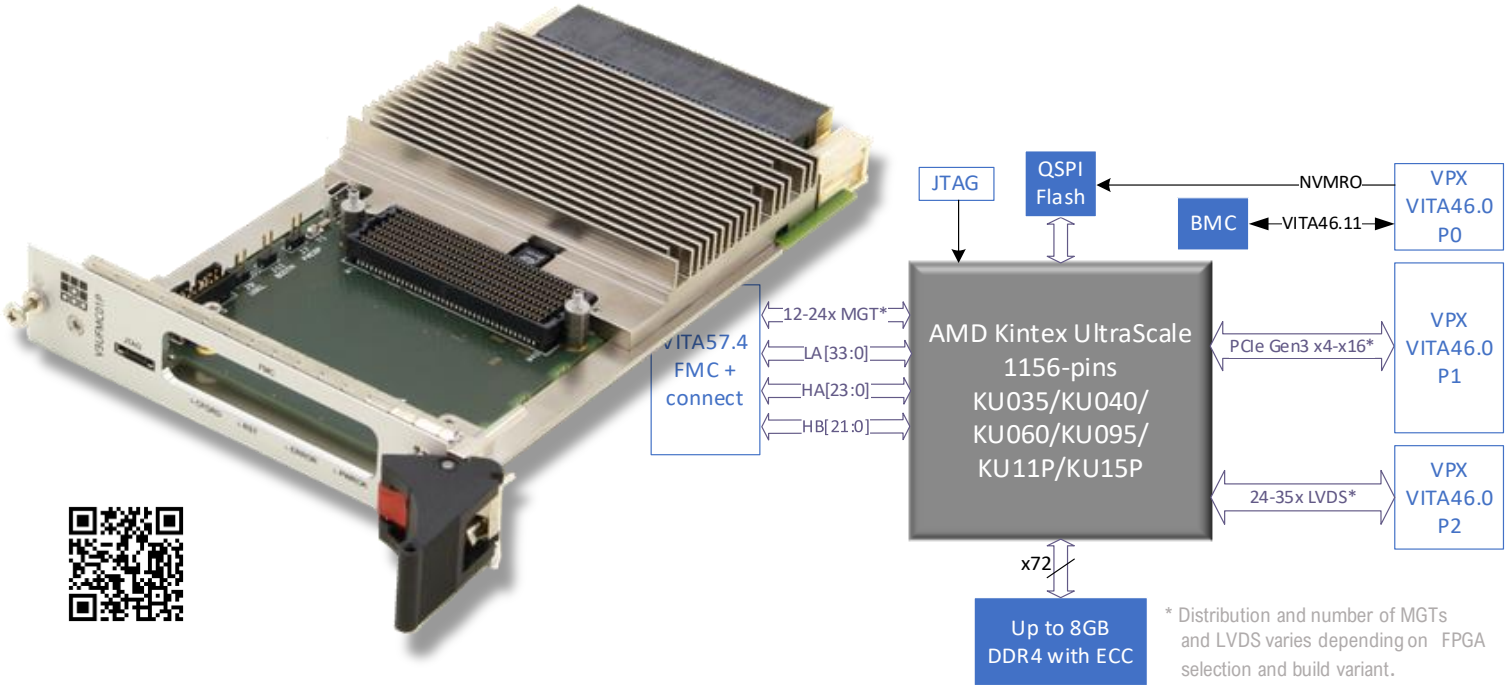
- **3U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard**
- **AMD® UltraScale™ FPGA processor**
- **Wide range of OpenVPX slot profiles**
- **Data & expansion planes for high-speed protocols**
- **Up to 8GB DDR4 ECC memory**
- **VITA 57.4 FMC+ mezzanine site for I/O module**
- **Air or conduction cooled**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**

DESCRIPTION

The 3U VPX V3UFMC01P is a member of Hybrid DSP's XU01P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the AMD Kintex UltraScale A1156 FPGA package, up to 8GB DDR4 and an ARM-based Board Management Controller (BMC).

The V3UFMC01P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include an FMC+ site to support mezzanine cards with I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.



url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Kintex UltraScale™ A1156 FPGA XCKU035, XCKU040, XCKU060, XCKU095, XQKU040, XQKU060, XQKU095**
- **DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 35 LVDS on VPX P2**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

Front Panel I/O
- **FMC+ site per VITA 57.4**
- **Extended component free region**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1" and 0.8"**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

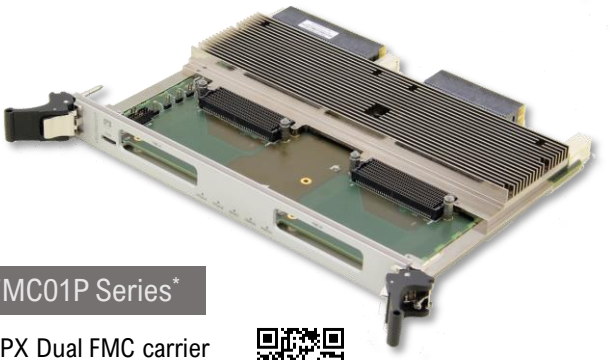
Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UADC01P Series*

- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock



V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFMC02P Series*

- 3U VPX FMC Carrier
- Based on **V3UFMC01P**
- Kintex UltraScale+ FPGA

V3UFMC51P Series*

- 3U VPX FMC Carrier
- High-end Series
- Virtex UltraScale+ 2104
- Roadmap Product

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

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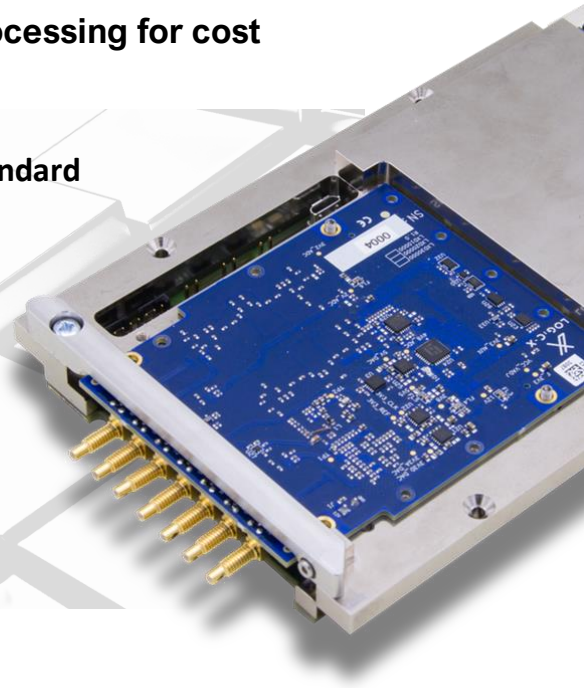
url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

V3UFT101P 5.4GSPS Low-Latency AD/DA

Rugged mid-range AMD UltraScale/UltraScale+ FPGA processing for cost sensitive defence, aerospace and industrial programs



- **3U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard**
- **AMD® UltraScale™ FPGA processor**
- **ADC 5.4Gsps 12-bits, 0.5 to 4800 MHz BW, 7.2 ns latency**
- **DAC 5.4Gsps 12-bits, 0.5 to 6000 MHz BW, 1.2 ns latency**
- **Data & expansion planes for high-speed protocols**
- **Up to 8GB DDR4 ECC memory**
- **Air or conduction cooled**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**

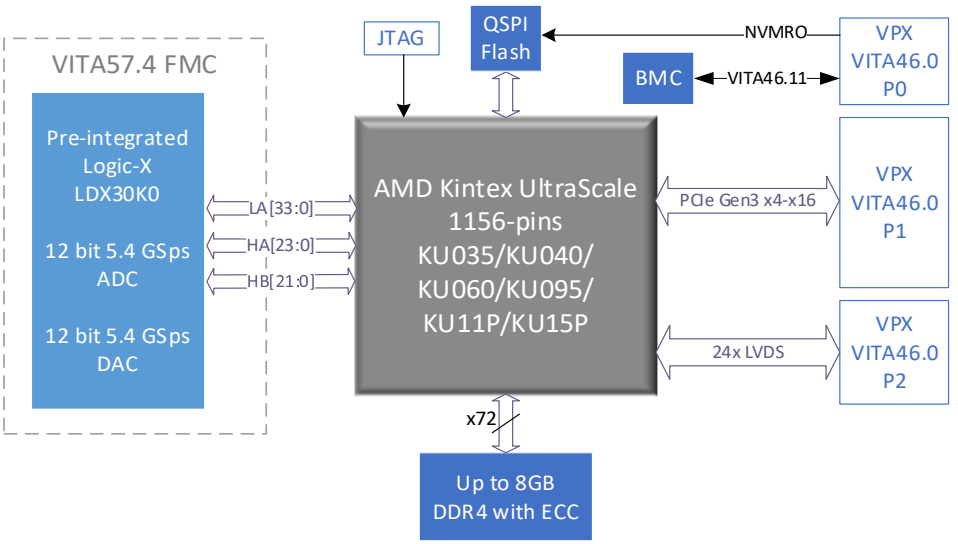
DESCRIPTION

The 3U VPX V3UFT101P is a member of Hybrid DSP's XU01P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the AMD Kintex UltraScale A1156 FPGA package, up to 8GB DDR4 and an ARM-based Board Management Controller (BMC).

The V3UFT101P offers a pre-integrated solution of a V3UFMC01P 3U VPX carrier board with the Logic-X LDX30K0 wide bandwidth, low-latency AD/DA FMC. A sample rate of 5.4Gsps coupled with an LVDS interface to the FPGA offers an extremely low-latency solution ideally suited for EW and radar applications.

The V3UFT101P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

The default solution, shown below, combines the V3UFMC01P4 with the LDX30K0. The V3UFMC01P4 provides an LVDS intensive VPX P2 configuration. A fully SOSA aligned solution, combining V3UFMC01P7 with the FMC is also available.



url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Kintex UltraScale™ A1156 FPGA XCKU035, XCKU040, XCKU060, XCKU095, XQKU040, XQKU060, XQKU095**
- **DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 35 LVDS on VPX P2**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

Front Panel I/O
- **ADC 5.4Gsps 12-bits, 0.5 to 4800 MHz BW, 7.2 ns latency**
- **DAC 5.4Gsps 12-bits, 0.5 to 6000 MHz BW, 1.2 ns latency**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1” and 0.8”**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

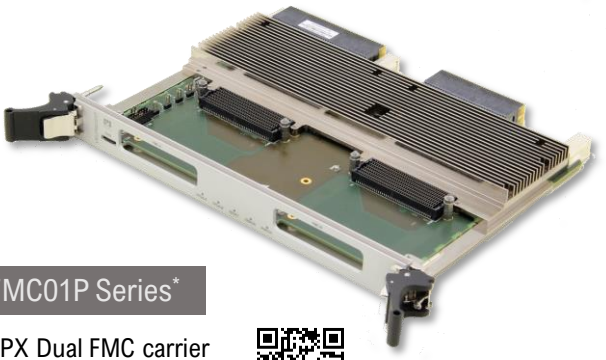
Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UADC01P Series*

- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock

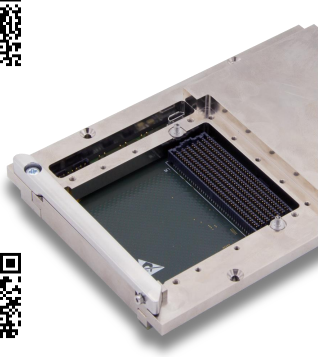


V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFMC02P Series*

- 3U VPX FMC Carrier
- Based on **V3UFMC01P**
- Kintex UltraScale+ FPGA



V3UFMC01P7*

- 3U VPX FMC Carrier
- Kintex UltraScale FPGA
- VITA 57.4 FMC+ Site
- P2B VITA67.3D profile
- Including 4 channel optical transceiver on P2B

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

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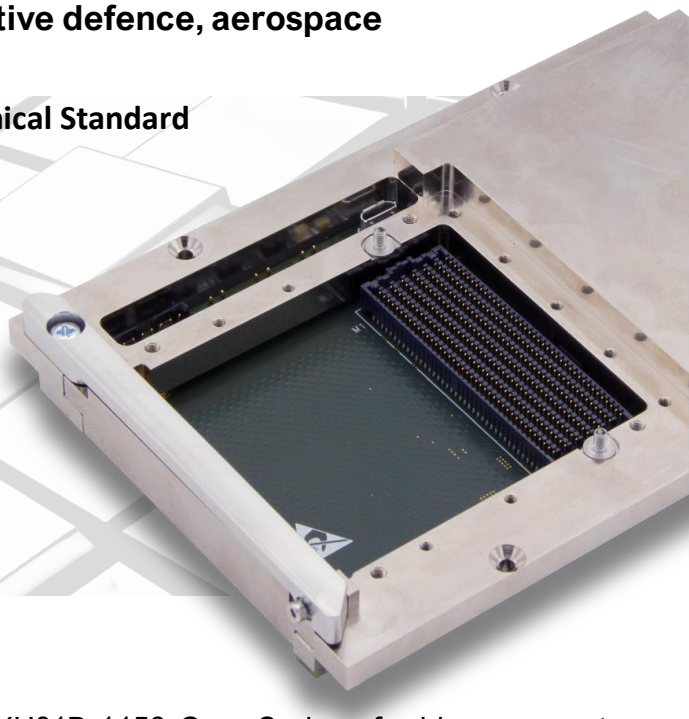
url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

V3UFMC01P7 AMD UltraScale FMC+ Carrier

Rugged mid-range FPGA processing for cost sensitive defence, aerospace and industrial programs

- **3U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard**
- **AMD® UltraScale™ or UltraScale+™ FPGA processor**
- **Wide range of OpenVPX slot profiles**
- **Data & expansion planes for high-speed protocols**
- **SOSA aligned, P2B VITA67.3D profile**
  - ***Light*CONEX® 4TRX Optical Module on-board**
  - **Up to 10 NanoRF from FMC**
- **Up to 8GB DDR4 ECC memory**
- **VITA 57.1 FMC mezzanine site for I/O module**
- **Air or conduction cooled**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**

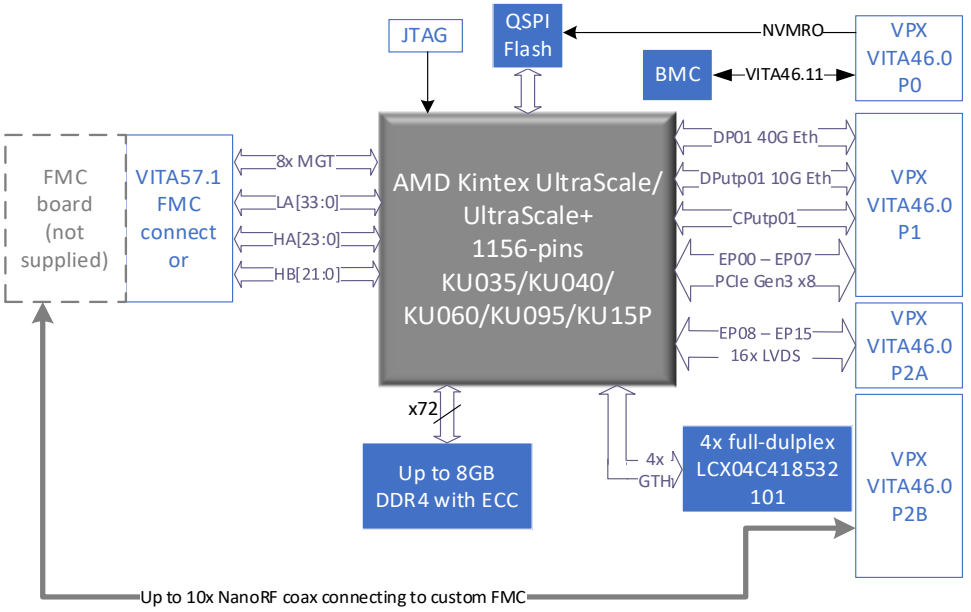


DESCRIPTION

The 3U VPX V3UFMC01P7 is a member of Hybrid DSP's XU01P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the AMD Kintex UltraScale A1156 FPGA package, up to 8GB DDR4 and an ARM-based Board Management Controller (BMC).

The V3UFMC01P7 is a SOSA aligned build option of the V3UFMC01P, providing a combined optical and coax interface in alignment with VITA 65.0 Payload Slot Profile SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13-4. The optical interface consists of 4 TX and 4 RX fibres, offering 40Gbps of bandwidth in each direction. Up to 10 NanoRF coax cables can be routed to any type of VITA 57.1 FPGA Mezzanine Card.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.



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email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Kintex UltraScale(+)™ A1156 FPGA XCKU035, XCKU040, XCKU060, XCKU095, XQKU040, XQKU060, XQKU095, KU15P**
- **DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-3 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **16 LVDS on VPX P2A (can be disconnected)**
- **4 TRX 10.3125Gbps optics on VPX P2B**
- **10 NanoRF to FMC on VPX P2B**

Front Panel I/O
- **FMC+ site per VITA 57.1**
- **Extended component free region**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1”**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

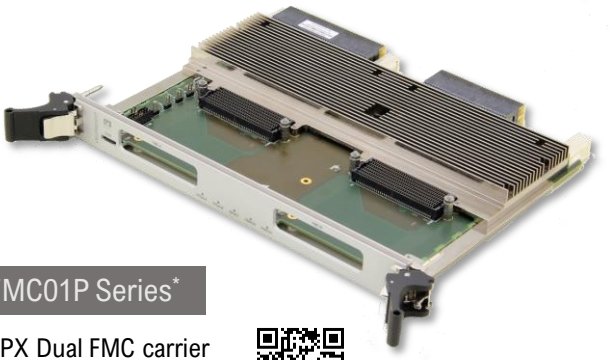
Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.1**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UADC01P Series*

- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock



V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFT101P Series*

- 3U VPX 5.4Gsps AD/DA
- Based on **V3UFMC01P**
- Kintex UltraScale+ FPGA

V3UFMC51P Series*

- 3U VPX FMC Carrier
- High-end Series
- Virtex UltraScale+ 2104
- Roadmap Product

SUPPORT AND VARIANTS

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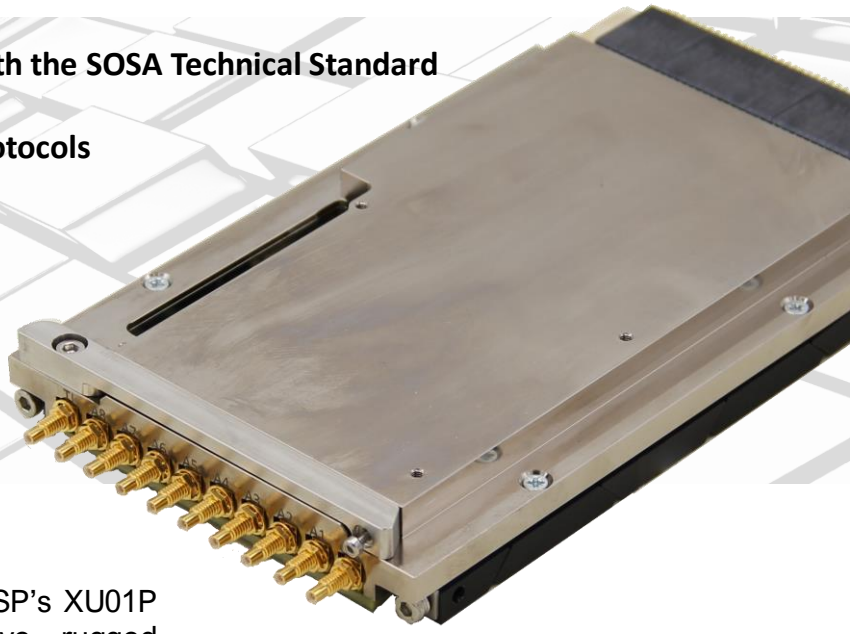
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

V3UADC01P AMD UltraScale 8CH ADC

Rugged mid-range FPGA data acquisition and processing for cost sensitive defence, aerospace and industrial programs

- **3U VPX Monolithic 8CH Digitizer aligned with the SOSA Technical Standard**
- **AMD® UltraScale™ FPGA processor**
- **Data & expansion planes for high-speed protocols**
- **Wide range of OpenVPX slot profiles**
- **Up to 8GB DDR4 ECC memory**
- **Analogue-to-Digital Convertor**
  - **8-channels 250Msps 14-bit ADC**
- **Air or conduction cooled**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**



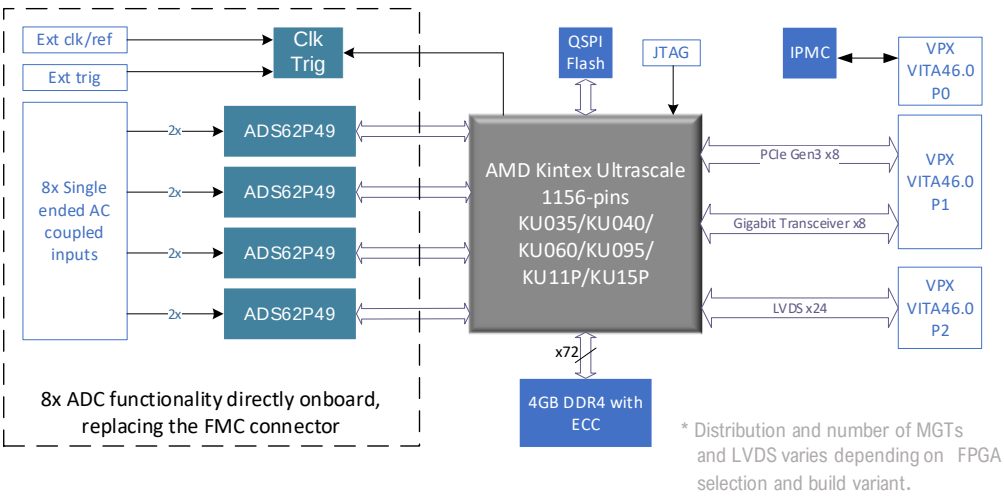
DESCRIPTION

The 3U V3UADC01P is a member of Hybrid DSP's XU01P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the AMD Kintex UltraScale A1156 FPGA package, up to 8GB DDR4 and an ARM-based Board Management Controller (BMC).

The V3UADC01P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include eight ADC channels running at up to 250Msps with coax on either the front panel or optionally VITA 67 coax blind mate connectors on the backplane. The board supports external and internal trigger and clock sources.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the type of coax connectors, front panel design, cooling solution, reference firmware, and BMC.

The monolithic V3UADC01P is based on the V3UFMC01P and a customer's legacy FMC ADC module. Hybrid DSP's Modified-COTS optimized base XU01P design permitted a low-risk, rapid form-fit-function replacement of the existing modular solution leading to simplification of supply-chain, lifecycle management and serviceability, as well as a significant cost-saving across the program lifetime.



* Distribution and number of MGTs and LVDS varies depending on FPGA selection and build variant.

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email: info@hybriddsp.nl
tel: +31 15 870 0817

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2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Kintex UltraScale™ A1156 FPGA XCKU035, XCKU040, XCKU060, XCKU095, XQKU040, XQKU060, XQKU095**
- **DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 35 LVDS on VPX P2**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 67 Coaxial options**

Analogue Front-End
- **8-channels 250Msps 14-bit ADC**
- **ENOB 10.8 bit, SFDR 84dBc**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1” and 0.8”**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

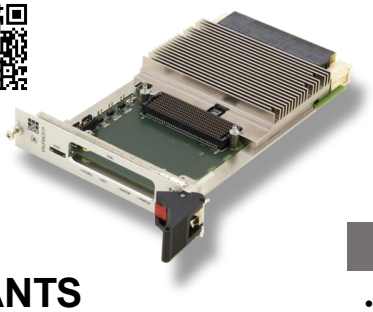
Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**

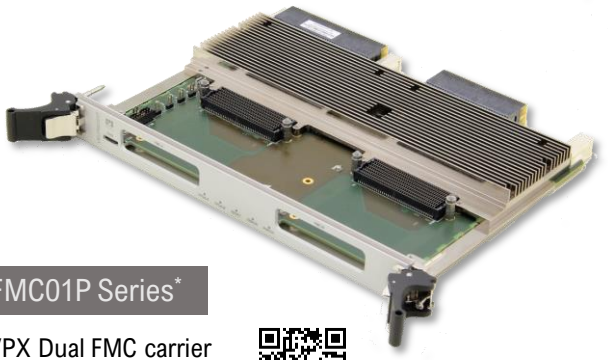
VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UFMC01P Series*

- 3U VPX FMC Carrier
- Kintex UltraScale FPGA
- VITA 57.4 FMC+ Site



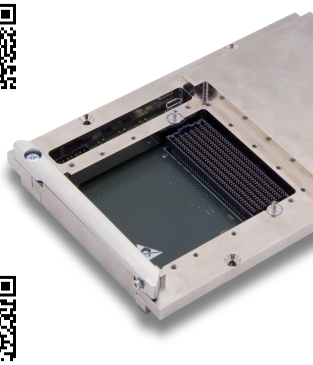


V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFMC02P Series*

- 3U VPX FMC Carrier
- Based on **V3UFMC01P**
- Kintex UltraScale+ FPGA



V3UFMC51P Series*

- 3U VPX FMC Carrier
- High-end Series
- Virtex UltraScale+ 2104
- Roadmap Product

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

Contact Hybrid DSP to discuss how we can accelerate your next development.

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email: info@hybriddsp.nl
tel: +31 15 870 0817

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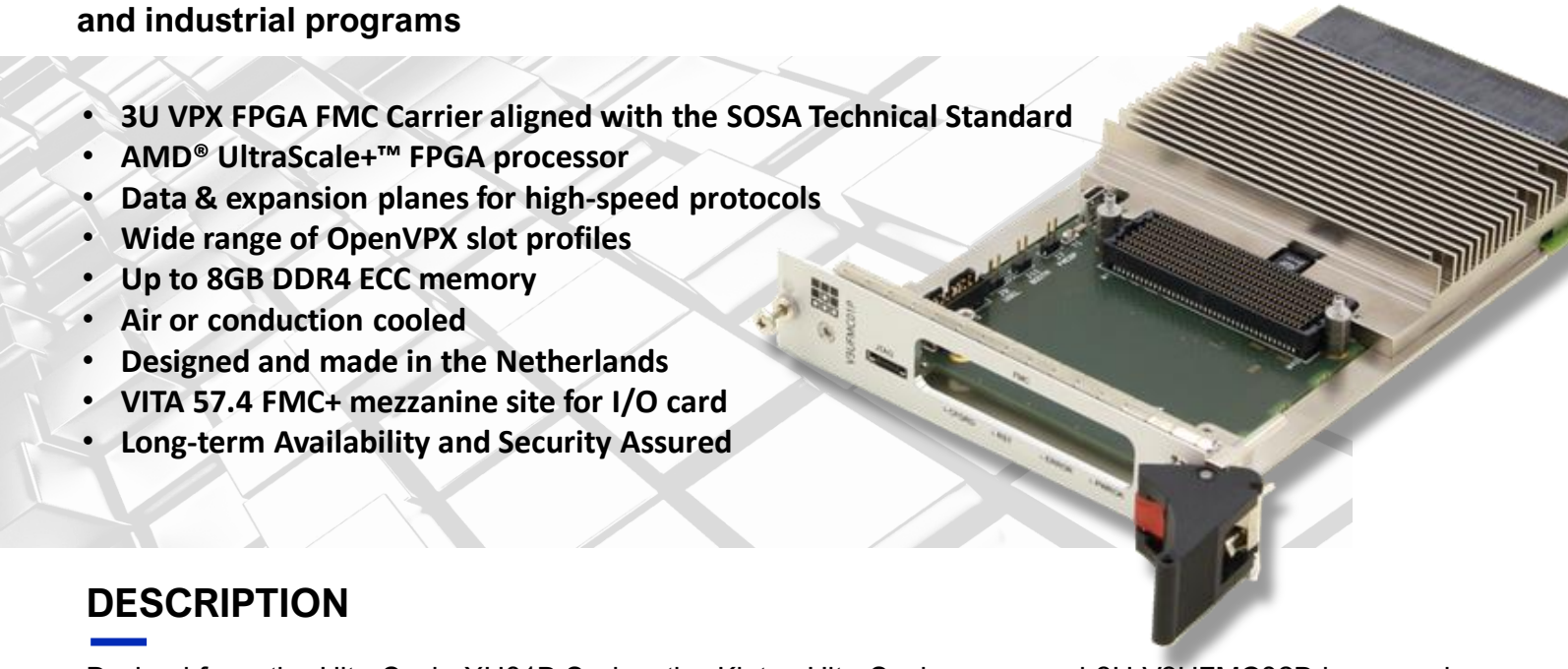
The Netherlands

V3UFMC02P AMD UltraScale+ FMC+ Carrier

Rugged mid-range FPGA processing for cost sensitive defence, aerospace and industrial programs



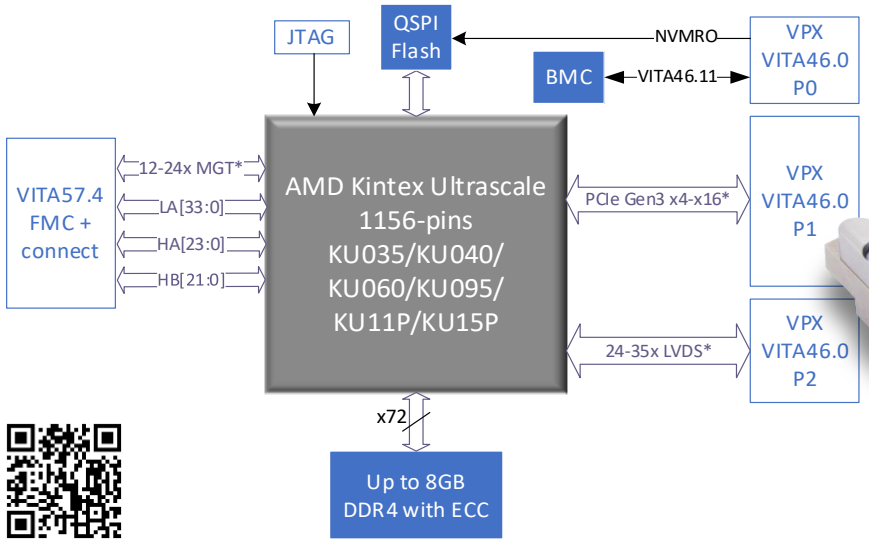
- **3U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard**
- **AMD® UltraScale+™ FPGA processor**
- **Data & expansion planes for high-speed protocols**
- **Wide range of OpenVPX slot profiles**
- **Up to 8GB DDR4 ECC memory**
- **Air or conduction cooled**
- **Designed and made in the Netherlands**
- **VITA 57.4 FMC+ mezzanine site for I/O card**
- **Long-term Availability and Security Assured**

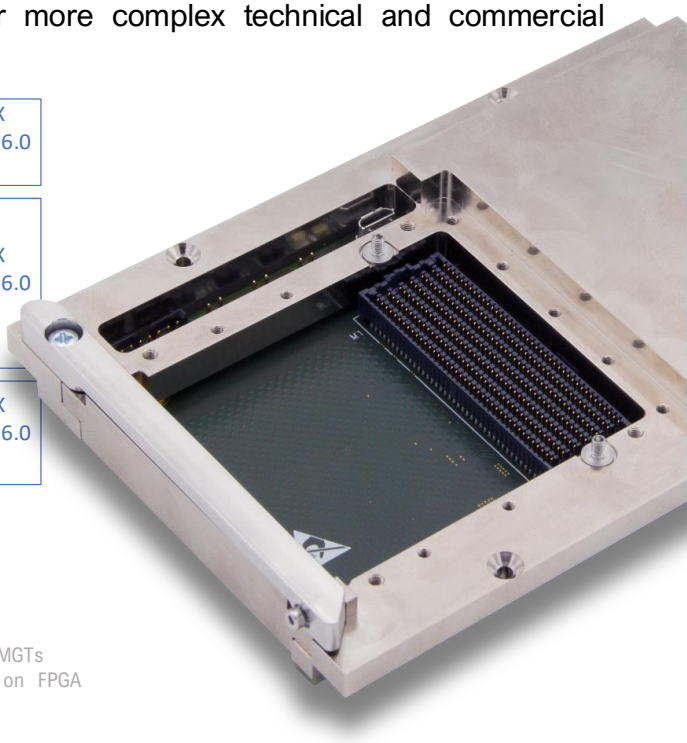
DESCRIPTION

Derived from the UltraScale XU01P Series, the Kintex UltraScale+ powered 3U V3UFMC02P is a member of Hybrid DSP's XU02P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the AMD Kintex UltraScale+ A1156 FPGA package, up to 8GB DDR4 and an ARM-based Board Management Controller (BMC).

The V3UFMC02P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include an FMC+ site to support mezzanine cards with I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.





* Distribution and number of MGTs and LVDS varies depending on FPGA selection and build variant.

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email: info@hybriddsp.nl
tel: +31 15 870 0817

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2321JW Leiden
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TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Kintex UltraScale+™ A1156 FPGA XCKU11P, XCKU15P**
- **DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 35 LVDS on VPX P2**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

Front Panel I/O
- **FMC+ site per VITA 57.4**
- **Extended component free region**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1" and 0.8"**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

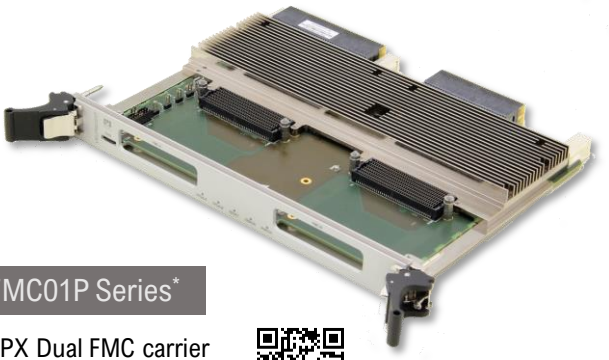
Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UADC01P Series*

- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock



V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFMC01P Series*

- 3U VPX FMC Carrier
- Kintex UltraScale FPGA
- VITA 57.4 FMC+ Site

V3UFMC51P Series*

- 3U VPX FMC Carrier
- High-end Series
- Virtex UltraScale+ 2104
- Roadmap Product

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

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email: info@hybriddsp.nl
tel: +31 15 870 0817

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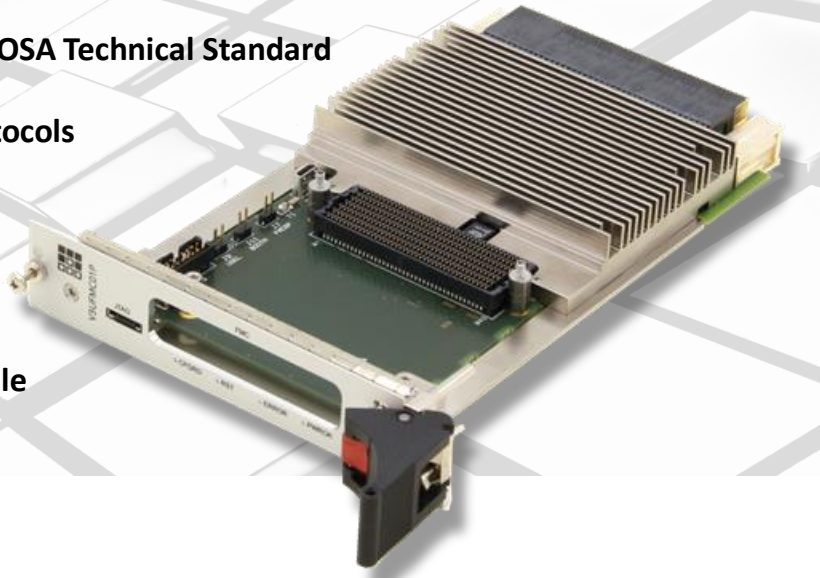
2321JW Leiden
The Netherlands

V3UFMC51P Virtex UltraScale+ FMC+ Carrier

Rugged high-end FPGA processing for demanding defence, aerospace and industrial programs

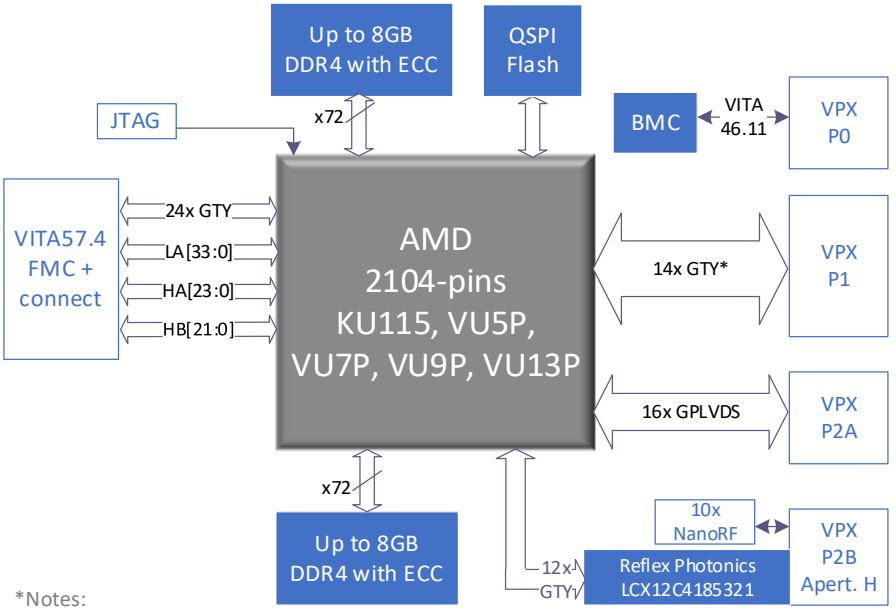
- **3U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard**
- **AMD® UltraScale+™ FPGA processor**
- **Data & expansion planes for high-speed protocols**
- **Wide range of OpenVPX slot profiles**
- **Up to 16GB DDR4 ECC memory**
- **Air or conduction cooled**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**
- **VITA 57.4 FMC+ mezzanine site for I/O module**

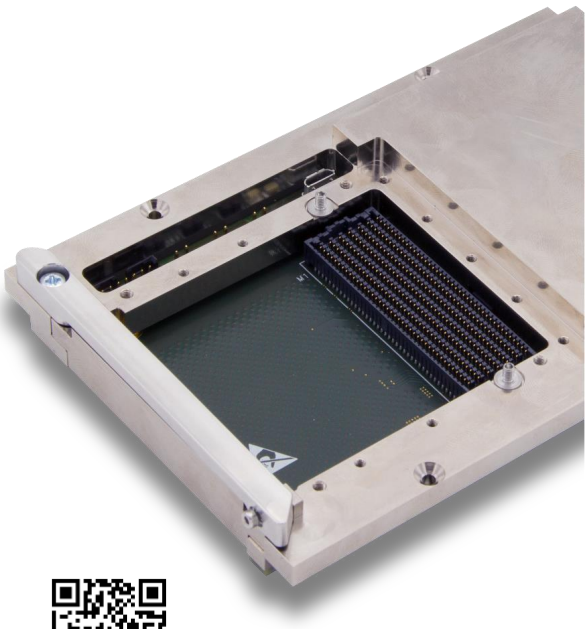


DESCRIPTION

The 3U V3UFMC51P is a member of Hybrid DSP's XU51P Series of high-end, rugged processing boards based on the AMD Virtex UltraScale+ A2104 FPGA package, up to 16GB DDR4 and an ARM-based Board Management Controller (BMC). The V3UFMC51P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include an FMC+ site to support mezzanine cards with I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.





*Notes:
- VPX P1.9 – P1.16 supports PCIe Gen3 2x4 or 1x8
- In alignment with SOSA PIC Profiles:
  MOD3-PAY-1F1U1S1S1U1U4F1J-16.6.13-3
  MOD3-PAY-1F1U1S1S1U1U4F1J-16.6.13-5

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

VPX™ SOSA Sensor Open Systems Architecture

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Virtex UltraScale+™ A2104 FPGA VU5P, VU7P, VU9P, V13P**
- **Dual DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (3U)
- **Up to 16 serial transceiver lanes on VPX P1 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 16 LVDS on VPX P2A**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

Front Panel I/O
- **FMC+ site per VITA 57.4**
- **Extended component free region**

Mechanical
- **3U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1" and 0.8"**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

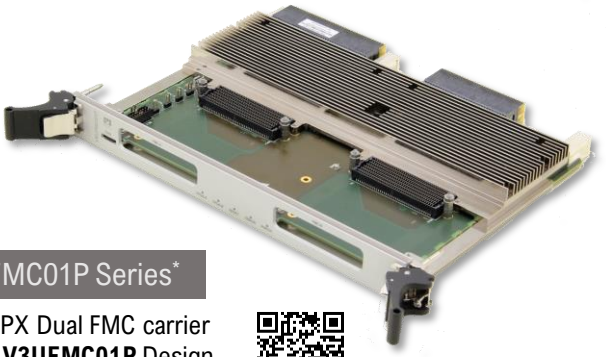
Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UADC01P Series*

- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock



V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

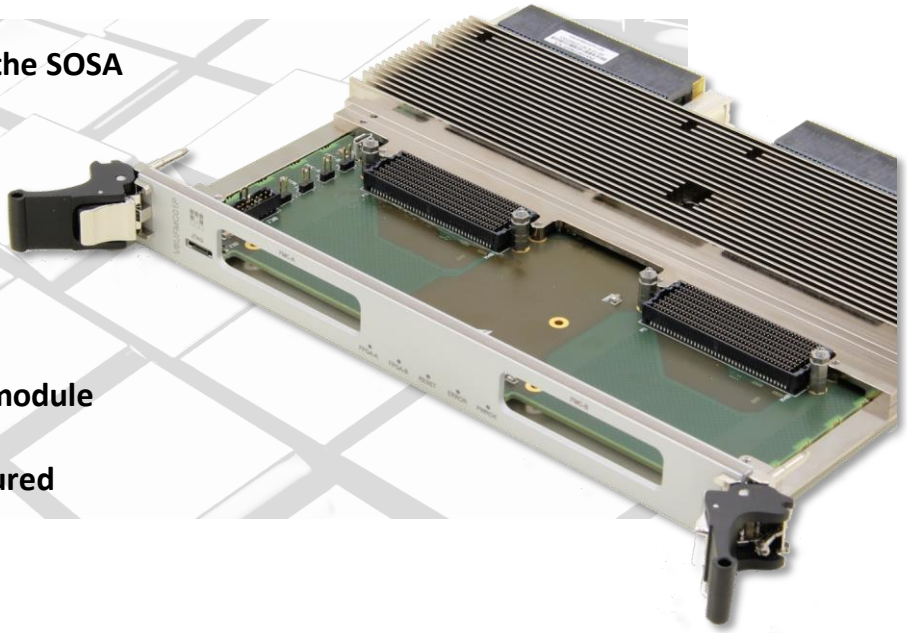
The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

Contact Hybrid DSP to discuss how we can accelerate your next development.

** Products and solutions were developed in alignment with the SOSA™ Technical Standard*

V6UFMC01P AMD UltraScale FMC+ Carrier

Rugged mid-range FPGA processing for cost sensitive defence, aerospace and industrial programs



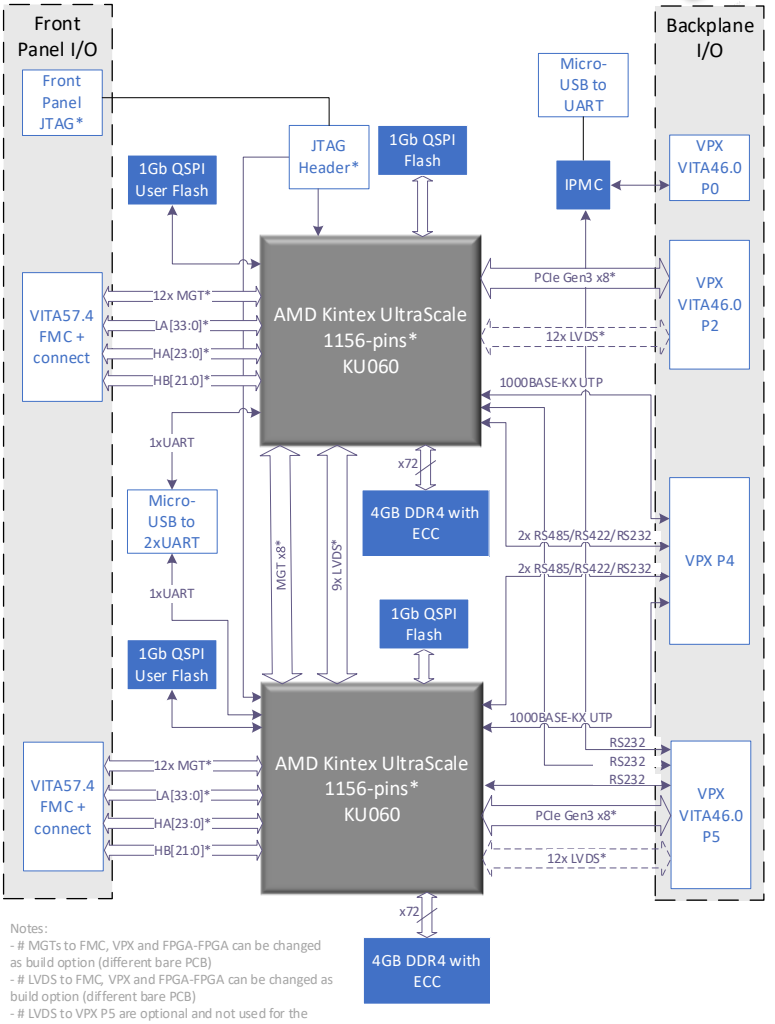
- 6U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard
- Data & expansion planes for high-speed protocols
- AMD® UltraScale™ FPGA processor
- Wide range of OpenVPX slot profiles
- Air or conduction cooled
- Up to 8GB DDR4 ECC memory per FPGA
- VITA 57.4 FMC+ mezzanine site for I/O module
- Designed and made in the Netherlands
- Long-term Availability and Security Assured

DESCRIPTION

The 6U V6UFMC01P is a member of Hybrid DSP's XU01P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the AMD Kintex UltraScale A1156 FPGA package, up to 8GB DDR4 per FPGA and an ARM-based Board Management Controller (BMC).

The V6UFMC01P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include two FMC+ sites to support mezzanine cards with I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.



Notes:
- # MGTs to FMC, VPX and FPGA-FPGA can be changed as build option (different bare PCB)
- # LVDS to FMC, VPX and FPGA-FPGA can be changed as build option (different bare PCB)
- # LVDS to VPX P5 are optional and not used for the first project
- Compatible with SOSA MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H- 12.6.4- 1
- KU060 is designed for, however KU040, KU11P and KU15P FPGAs could be permitted as build option
- Front panel JTAG and on-board JTAG header are both accessible but operate mutually exclusive

* V6UFMC01P**1** shown above
V6UFMC01P**2** has MGT x4 inter-FPGA and additional MGT x4 to P2 and P5

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Kintex UltraScale™ A1156 FPGA XCKU035, XCKU040, XCKU060, XCKU095, XQKU040, XQKU060, XQKU095**
- **DDR4 4GB or 8GB with ECC**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (6U)
- **Up to 12 serial transceiver lanes on VPX P2 and P5 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 12 LVDS on VPX P2 and P5**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

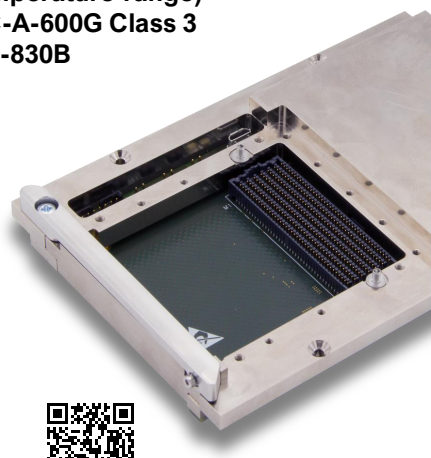
Front Panel I/O
- **Two FMC+ sites per VITA 57.4**
- **Extended component free region**

Mechanical
- **6U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1" and 0.8"**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**



RELATED PRODUCTS

V3UADC01P Series*

- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock

V3UFMC01P Series*

- 3U VPX FMC Carrier
- Kintex UltraScale FPGA
- VITA 57.4 FMC+ Site

V3UFMC02P Series*

- 3U VPX FMC Carrier
- Based on **V3UFMC01P**
- Kintex UltraScale+ FPGA

V3UFMC51P Series*

- 3U VPX FMC Carrier
- High-end Series
- Virtex UltraScale+ 2104
- Roadmap Product

SUPPORT AND VARIANTS

Hybrid DSP Systems supports her customers in the specification, design, production, integration and long-term product and life-cycle management of high-end rugged COTS and Modified-COTS 3U/6U VPX payload and I/O boards for VPX and OpenVPX based systems as well as those aligned with the SOSA Technical Standard.

Security of design and supply chain is increasingly important: the boards, firmware and software are designed and produced in the Netherlands. The Board Management Controller with VITA 46.11 IPMI is an in-house source available implementation.

The processes and IP used to design, produce and support her range of COTS products are fully modular and can be licensed on a flexible basis. Backed by discrete professional support and delivered and regularly updated in a transparent, traceable manner via private git repositories, the IP includes everything from complete board designs to source code and from mechanical files to documentation.

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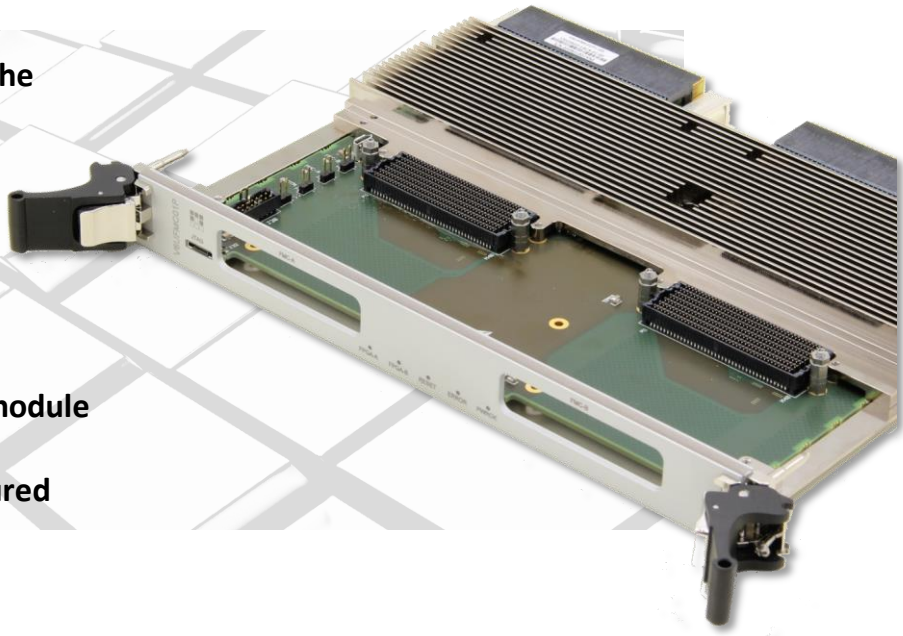
** Products and solutions were developed in alignment with the SOSA™ Technical Standard*

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
The Netherlands

V6UFMC02P AMD UltraScale+ FMC+ Carrier

Rugged mid-range FPGA processing for cost sensitive defence, aerospace and industrial programs



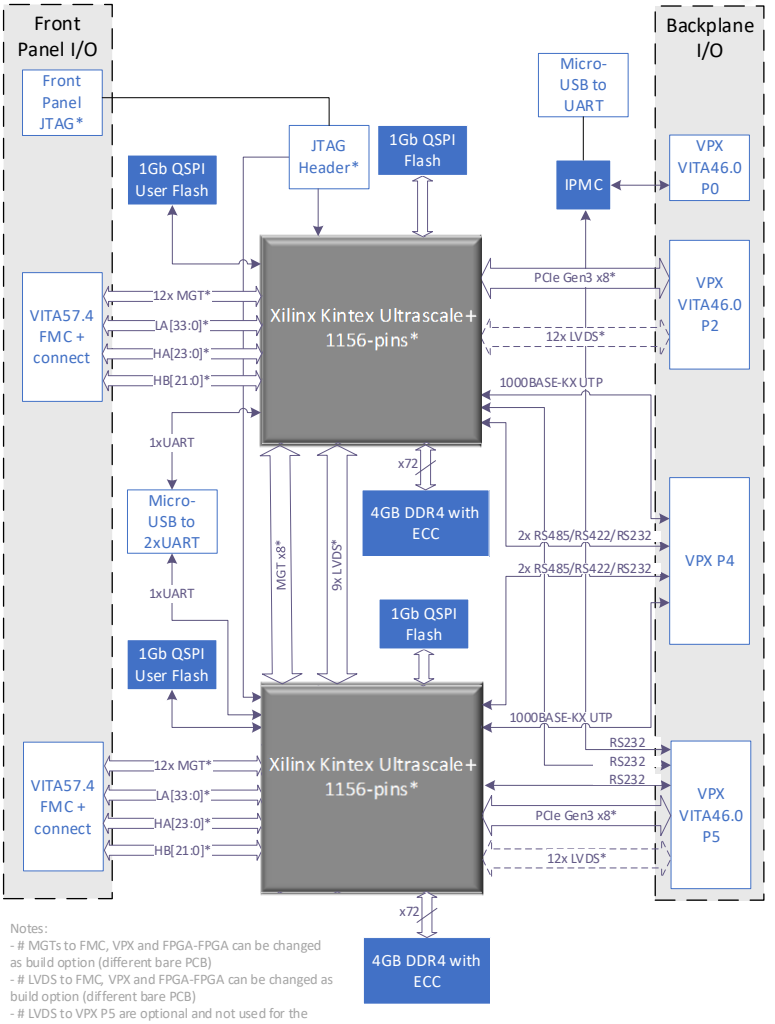
- **6U VPX FPGA FMC Carrier aligned with the SOSA Technical Standard**
- **Data & expansion planes for high-speed protocols**
- **AMD® UltraScale+™ FPGA processors**
- **Wide range of OpenVPX slot profiles**
- **Air or conduction cooled**
- **Up to 8GB DDR4 ECC memory per FPGA**
- **VITA 57.4 FMC+ mezzanine site for I/O module**
- **Designed and made in the Netherlands**
- **Long-term Availability and Security Assured**

DESCRIPTION

The 6U V6UFMC02P is a member of Hybrid DSP's XU02P 1156 Core Series of mid-range, cost effective, rugged processing boards based on the AMD Kintex UltraScale+ A1156 FPGA package, up to 8GB DDR4 per FPGA and an ARM-based Board Management Controller (BMC).

The V6UFMC02P is available with a range of build options for OpenVPX air and conduction cooled based systems as well as those aligned with the SOSA Technical Standard. Features include two FMC+ sites to support mezzanine cards with I/O routing to either the front panel or optionally VITA 66/67 optical/coax blind mate connectors on the backplane.

In addition to numerous standard build options, the design is optimized for rapid customization of many key features including the front-panel, cooling solution, reference firmware, and BMC. Furthermore, the PCB layout and stack-up allows for a viable low-risk route for more complex technical and commercial requirements including modular-to-monolithic.



Notes:
- # MGTs to FMC, VPX and FPGA-FPGA can be changed as build option (different bare PCB)
- # LVDS to FMC, VPX and FPGA-FPGA can be changed as build option (different bare PCB)
- # LVDS to VPX P5 are optional and not used for the first project
- Compatible with SOSA MOD6-PAY-4F2Q1H4U1T1S1S1TU2U2T1H- 12.6.4- 1
- KU060 is designed for, however KU040, KU11P and KU15P FPGAs could be permitted as build option
- Front panel JTAG and on-board JTAG header are both accessible but operate mutually exclusive

* V6UFMC02P**1** shown above
V6UFMC02P**2** has MGT x4 inter-FPGA and additional MGT x4 to P2 and P5

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

Kanaalpark 157
2321JW Leiden
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TECHNICAL SPECIFICATIONS

Main Processor and Memory
- **AMD Kintex UltraScale+™ A1156 FPGA XCKU11P, XCKU15P (Dual)**
- **DDR4 4GB or 8GB with ECC (per FPGA)**

Board Management
- **Voltage and temperature monitor**
- **Power/reset control**
- **Tier-2 VITA 46.11 IPMI**

Backplane Architecture (6U)
- **Up to 12 serial transceiver lanes on VPX P2 and P5 (PCIe Gen3, Aurora, Ethernet, RapidIO etc)**
- **Up to 12 LVDS on VPX P2 and P5**
- **VITA 65.0 and SOSA aligned slot profiles**
- **VITA 66/67 Optical and Coaxial options**

Front Panel I/O
- **Two FMC+ sites per VITA 57.4**
- **Extended component free region**

Mechanical
- **6U VPX COTS and Custom air- and conduction-cooled (FMC+) compatible heat-frame**
- **OpenVPX and VPX-REDI**
- **Pitch: 1” and 0.8”**

Board Support Package
- **Vivado project, VHDL based reference designs, UART and PCIe drivers, API, Python and C/C++ sample applications**

Compliance
- **OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.7, 46.9, 46.11**
- **Compatible with VITA 65 and SOSA aligned systems**
- **VITA 47.0**
- **VITA 48.0/48.1/48.2 (REDI)**
- **VITA 57.4**

VITA 47.0 Construction, Safety and Quality
- **Environmental Class: EAC1, EAC6, ECC1 and ECC3 (-40°C to +70°C operating temperature range)**
- **IPC-A-610D Class 3 and IPC-A-600G Class 3**
- **Conformal Coating: IPC-CC-830B**

RELATED PRODUCTS

V3UADC01P Series*

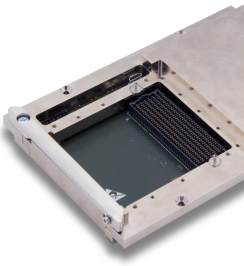
- 3U VPX Monolithic ADC
- Based on **V3UFMC01P** Design
- 8-channel 250Msps ADC
- Internal and external clock

V6UFMC01P Series*

- 6U VPX Dual FMC carrier
- Kintex UltraScale FPGA
- Dual **V3UFMC01P** Design
- Dual VITA 57.4 FMC+ Site

V3UFMC01P Series*

- 3U VPX FMC Carrier
- Kintex UltraScale FPGA
- VITA 57.4 FMC+ Site



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Kanaalpark 157
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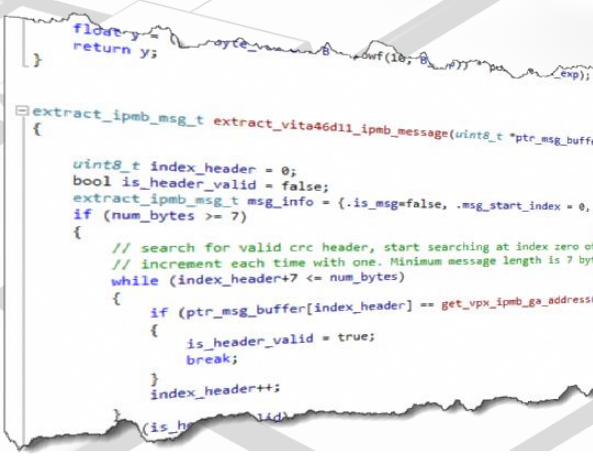
VITA 46.11 Tier 3 IPMC

A readily maintainable and customizable BMC implementation with VITA 46.11 Tier 3 support for 3rd party board developments

- **VITA 46.11-2022 Tier 3 compliant IPMC software core**
- **Up to Tier 3 in alignment with SOSA Technical Standard**
- **Redundant IPMB interface**
- **Lightweight bare-metal C implementation, portable to RTOS**
- **Source code available**
- **Developed inhouse by Hybrid DSP in the Netherlands**
- **SDR and FRU compiler utilities**
- **Reference designs for easy customer integration**
- **Free evaluation designs available**
- **Extensive documentation including Quick Start Guides**
- **Deliverables through GIT or a secured file transfer**



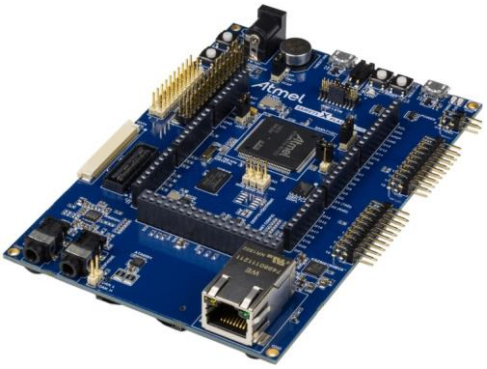
DESCRIPTION

The VITA 46.11-2022 software IP core implements all requirements defined for a Tier 3 IPMC. Typical target platforms of this software core are OpenVPX and SOSA aligned payload modules which interface to a Chassis Manager through the IPMB interfaces on the backplane.

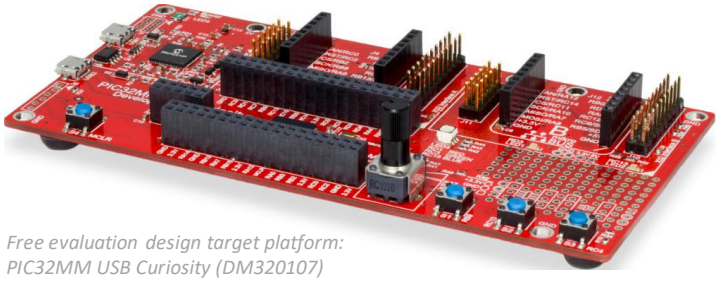
The bare-metal C implementation is lightweight and supports various microcontroller architectures such as ARM, PIC32 and RISC-V. Functions that make use of dedicated microcontroller peripherals are provided as part of reference designs, for example the I2C controller of the Microchip SAMV71 or the PIC32MM. Other microcontroller designs can be made available on request.

The IP core is delivered with an FRU (Field Replaceable Unit) and an SDR (Sensor Data Record) compiler utility. The SDR compiler takes sensor values and thresholds provided by the customer using the delivered SDR excel template. It generates required SDR data to be uploaded to the flash of the IPMC. Different output formats are available supporting standard file formats such as .hex and .bin, suitable for automated programming during board production.

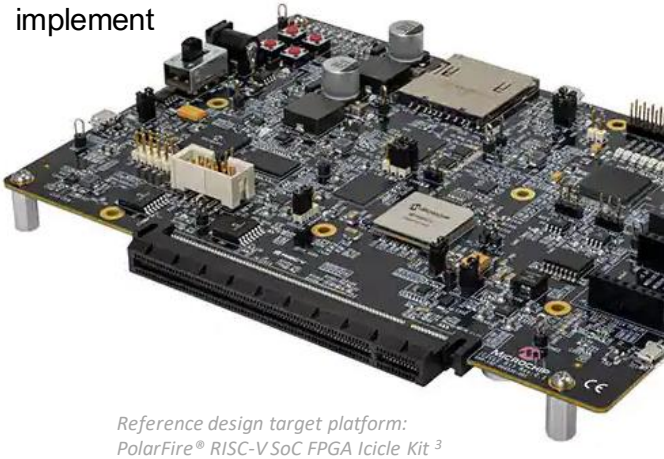
Hybrid DSP provides support with integration or can fully implement customers board management and IPMC functionality.



Free evaluation design target platform: SAMV71 Explained Ultra



Free evaluation design target platform: PIC32MM USB Curiosity (DM320107)



Reference design target platform: PolarFire® RISC-V SoC FPGA Icicle Kit [3]

url: hybriddsp.eu
email: info@hybriddsp.nl
tel: +31 15 870 0817

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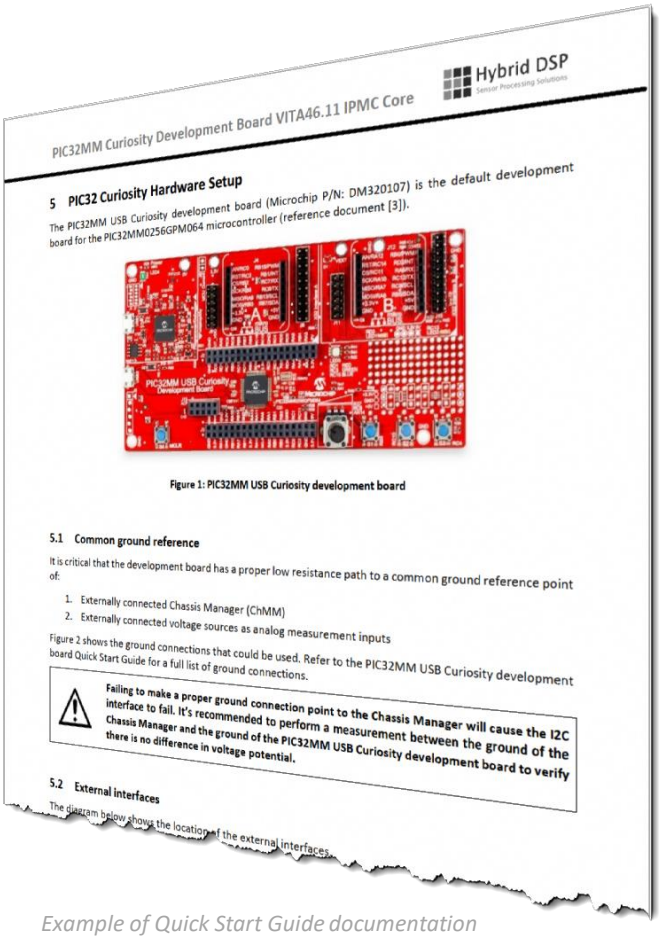
VITA 46.11 IPMC IP core and board management

Hybrid DSP
Sensor Processing Solutions

DELIVERABLES

- VITA 46.11 IPMC libraries or source code
- Reference design
- SDR converter utility with templates
- FRU compiler with templates
- Documentation
- Provided as archive via secured file transfer, or customer facing private GIT repository for optimized version control (Clone, Fetch, Pull, Push)


PIC32MM Curiosity Development Board VITA46.11 IPMC Core

Hybrid DSP

5 PIC32 Curiosity Hardware Setup

The PIC32MM USB Curiosity development board (Microchip P/N: DM320107) is the default development board for the PIC32MM0256GPM064 microcontroller (reference document [3]).

Figure 1: PIC32MM USB Curiosity development board

5.1 Common ground reference

It is critical that the development board has a proper low resistance path to a common ground reference point of:

1. Externally connected Chassis Manager (ChMM)
2. Externally connected voltage sources as analog measurement inputs

Figure 2 shows the ground connections that could be used. Refer to the PIC32MM USB Curiosity development board Quick Start Guide for a full list of ground connections.

Failing to make a proper ground connection point to the Chassis Manager will cause the I2C interface to fail. It's recommended to perform a measurement between the ground of the Chassis Manager and the ground of the PIC32MM USB Curiosity development board to verify there is no difference in voltage potential.

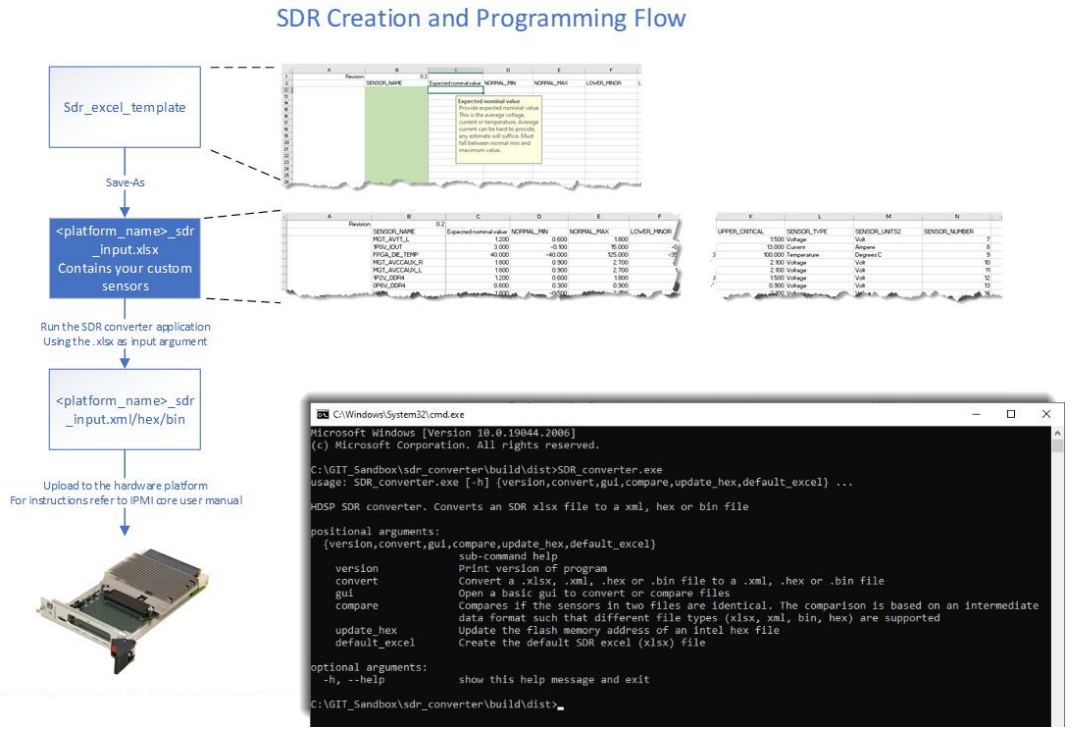
5.2 External interfaces

The diagram below shows the location of the external interfaces.

Example of Quick Start Guide documentation

REFERENCE DESIGNS

- Free evaluation designs available for:
  - Microchip ATSAMV71-XULT, ARM
  - Microchip DM320107, PIC32
- Including benchmarking/profiling results
- Command Line Interface (CLI) through UART
- Redundant IPMB connection to Chassis Manager
- GA and NVMRO pin settings can be configured through CLI
- Threshold sensor values can be emulated through CLI to test event generation
- Quick Start Guide providing instructions to connect to Chassis Manager and get started with the software
- Ipmitool docker image with example use cases
- Custom BMC and IPMI reference and production designs available on request



Instructions embedded in SDR .xlsx template

SDR AND FRU UTILITIES

- SDR Spreadsheet .xlsx template permits addition of custom sensors without in-depth VITA 46.11 knowledge
- FRU .xml template to generate the minimum FRU data required by VITA 46.11
- Command line SDR and FRU converter generating .bin or Intel .hex files that can be uploaded through the standard IDE programming interfaces or a customer specific interface
- SDR and FRU compilers delivered as Windows Executables

git

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